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Surface Charge Sensitivity of Silicon Nanowires: Size Dependence

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ABSTRACT

Silicon nanowires of different widths were fabricated in silicon on insulator (SOI) material using conventional process technology combined with electron-beam lithography. The aim was to analyze the size dependence of the sensitivity of such nanowires for biomolecule detection and for other sensor applications. Results from electrical characterization of the nanowires show a threshold voltage increasing with decreasing width. When immersed in an acidic buffer solution, smaller nanowires exhibit large conductance changes while larger wires remain unaffected. This behavior is also reflected in detected threshold shifts between buffer solutions of different pH, and we find that nanowires of width >150 nm are virtually insensitive to the buffer pH. The increased sensitivity for smaller sizes is ascribed to the larger surface/volume ratio for smaller wires exposing the channel to a more effective control by the local environment, similar to a surrounded gate transistor structure. Computer simulations confirm this behavior and show that sensing can be extended even down to the single charge level.

Semiconductor nanowires and (semiconducting) carbon nanotubes have been reported as promising building blocks for future biosensors enabling direct electrical detection of biomolecules.[1−4] The small size or, more specifically, the small diameter, typically below 50 nm, causes their electrical properties to be very dependent on the local environment where charge changes on the surface induce a field effect that significantly changes the carrier concentration and thus, the conductance. This charge sensitivity is in principle not limited to the surface of the device but is usually set by the Debye screening length in the liquid which could be on a nanometer range at high molar concentrations. The sensitivity of nanowires for biomolecule detection has been shown to extend down to the attomolar range[5] although single-molecule detection has (to authors knowledge) not yet been observed.

The electrical characteristics of low- to medium-doped nanowires resemble that of field effect transistors where a channel is induced (or depleted) in the nanowire depending on the local charge and on the bias of an external gate.[6,7] Doping of the nanowire plays here a minor role and whether electrons or holes are the active current carrying species is effectively determined by the contacts to the nanowire. The high sensitivity for local charges also has a parallel in conventional silicon technology where MOS transistors are sensitive to charges in the gate oxide largely affecting their threshold behavior. Indeed, at very small channel dimensions, this can be extended down to the single charge level, as demonstrated at room temperature in the 1990s.[8]

Up to now, most reports of nanowires as biosensors have been based on nanowires grown in the gas phase by CVD techniques that were subsequently deposited onto silicon wafers. The wafers had an insulating top oxide and contacts were either patterned before deposition or after. The first method relies on a random alignment of nanowires between contacts, whereas the second method involves inspection with SEM and subsequent lithography. Both methods involve a large randomness in fabrication and do not seem to be easily scalable for mass fabrication and for multiple detection devices involving a large number of sensors. The advantage of the technique, on the other hand, is the relative ease of production of small diameter nanowires of very homogeneous width.

Recent reports have, however, pointed out the possibility to use ordinary silicon CMOS technology to achieve similar effects.[1,9] The nanowire is then defined in the active top layer of a SOI wafer (silicon on insulator) thinned down to the order of ∼100 nm and contacts are formed using conventional metallization schemes. The small width, crucial to the sensitivity, is achieved by electron-beam lithography but may

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eventually be defined using deep UV lithography as CMOS technology move into the sub-50 nm range.

Modeling of the electrical behavior of silicon nanowires is difficult because size and geometry may not be known accurately, including, e.g., oxide charges. As a result, simple surface charge arguments or even changes in the mobility at small diameters have been invoked.[9,10] Thus, the large sensitivity of small-diameter nanowires for local charges compared to large devices has not been explained.[11,12] This would require full three-dimensional simulations, including relevant built-in charges of all surfaces of the nanowire.

In this work, we address the size dependence of the sensitivity of silicon nanowires for local charge changes as, e.g., during biomolecule detection. We have therefore fabricated nanowires of different widths (including a micrometer-sized wire) on the same chip to be able to compare electrical characteristics as a function of only nanowire width under equal processing conditions. The nanowires were defined in SOI material using electron-beam lithography, while large silicon leads and contacts were defined using optical lithography. Electrical characteristics were studied both for as-fabricated wires and under buffer solutions of pH = 3.0 and 7.4 to positively charge the amino groups (and negatively charge remaining silanol groups) on the nanowire surface and thus change the electrical properties of the device.[4] Our measurements and extraction of threshold voltages for the different sizes are supported by simulations of the cross-sectional charge density in the nanowire at different surface charge concentrations. This enables us to demonstrate the superior charge sensitivity as the nanowire width is reduced, in fact approaching the single charge level as demonstrated previously for narrow-channel MOS devices.

Nanowires were fabricated on silicon on insulator (SOI) material using e-beam lithography and optical lithography followed by plasma etching. Their widths were varied using different dose in the e-beam lithography process, thus creating an opening in the resist of different size. The top silicon layer was 100 nm thick (p-doped, $\rho = 17-22\ \Omega$ cm) separated through a 400 nm thick buried oxide layer from the bulk silicon. The nanowires were oxidized in a dry oxidation process at 900 °C for 10 min (nominally resulting in a 5 nm thick oxide) to provide electrical isolation and to increase the stability and decrease the number of dangling bonds. After oxidation, the nanowire surface was modified with APTES molecules that react with the −SiOH groups on the surface, resulting in an $-NH_2$ surface termination. Two buffer solutions were used, 40 mM NaOAc with pH = 3.0 and 10 mM $NaPO_4$ with pH = 7.4. A top view of the chip layout can be found in Figure 1 a. The 22 gold pads (0.2 μm thick) to the right connect to the 20 nanowires to the left. The gold wires connect to 100 μm wide Si pads, which are in connection to the nanowires shown in Figure 1b. The nanowire width was varied from ~50 to ~170 nm, and the length was 1 μm for all of them. A SEM image of a typical nanowire is shown as inset in Figure 3. Two microwires were included on all chips next to the nanowires.

For electrical characterization, a computer-controlled picoammeter/voltage source (Keithley 6487) and a KPCI-3201 D/A−A/D card was used. A voltage, $V_{DS} = V_D - V_S$, was applied between the source and the drain of the nanowire and another voltage, $V_{GS} = V_G - V_S$, was applied to the bulk Si layer working as a back gate.

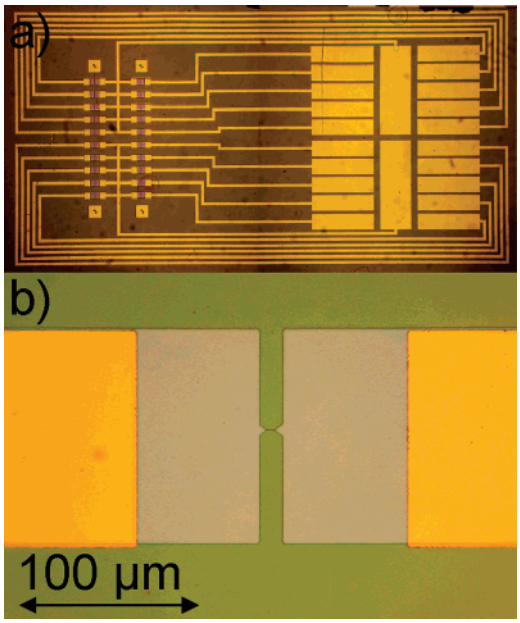

Figure 1. Optical micrographs of a silicon nanowire chip, 10 mm long. (a) Full chip with gold contact pads to the right and gold interconnects to the Silicon nanowires to the left. (b) Detail showing the Schottky junction contact area (TiW/Au) partly covering the silicon leads connected to the nanowire in the center.

The electrical properties of the nano- and microdevices were simulated in a two-dimensional semiconductor simulation package (ISE-TCAD). The devices were simulated in a cross section perpendicular to the wires.

We have previously reported[13] that the nanowires work in a similar way as MOS transistors, conducting through an inversion layer close to the silicon dioxide layer. Typical $I_{DS}-V_{DS}$ curves from such a device are shown in Figure 2a. Different saturation currents, I_{DS} (sat), are observed for different back gate voltages, V_{GS}, which confirm the MOS behavior. However, for smaller nanowires, $w < \sim 140$ nm, there is a quenching of the channel due to surface charges at low V_{DS} bias also seen before.[14] This is due to surface charges blocking the channel, and this behavior is increased with decreasing width.[15] For intermediate-sized nanowires, 140 nm $< w <$ 160 nm, the $I_{DS}-V_{DS}$ characteristics are similar to a MOS transistor. This also confirms that the Schottky junctions at the contacts do not limit the current through the device (largely because of the large contact area). For larger wires, $w > \sim 140$ nm, at high gate voltage and high bias, there is a limit in the current due to the Schottky junctions.[15] Based on the contact area, 100 μm × 100 μm, the Schottky barrier between Ti/W and Si, $\Phi_B = 0.46$ eV, and room temperature, $T = 300$ K, using the standard Schottky current formula, this current can be calculated to ~20 μA. In our nanowires and microwire, the limiting current amounts to ~0.5 μA, possibly due to the entire contact area not being active (injection closer to nanowires should dominate).

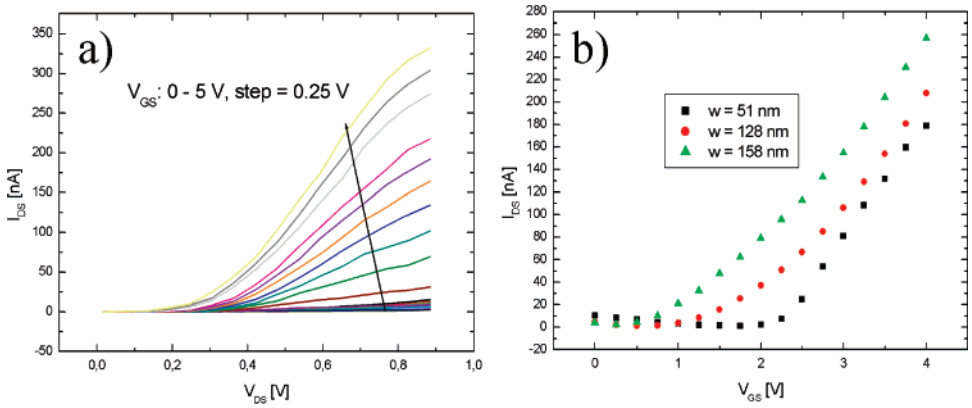

Figure 2. (a) Typical $I_{DS}-V_{DS}$ curves for a nanowire ~50 nm wide at different back gate voltages V_{GS}: 0−5 V, step = 0.25 V. (b) I_{DS} vs V_{GS} for three different nanowires of widths 51, 128, and 158 nm extracted from $I_{DS}-V_{DS}$ curves of each nanowire respectively at V_{DS} = 0.77 V.

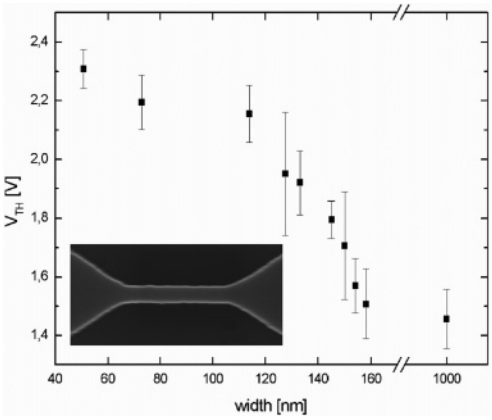

Figure 3. Threshold voltage plotted vs width for nanowires of 50−160 nm width and for one microwire of ~1 μm width. The threshold voltage has been extrapolated from $I_{DS}-V_{GS}$ plots[16] at 0.77 V (error bars show variation in fits). Inset shows a top SEM image of a typical nanowire of 154 nm width.

To measure the sensitivity of such a device a crucial parameter is the threshold voltage, V_{TH}. A change of surface charges should either enhance the current (positive charges) or decrease the current (negative charges) and thus work as a top gate. As a result, the threshold voltage for the back gate, V_{GS}, would be changed. Moreover, at small widths, surface charges on the sidewall of the nanowires will become increasingly important, influencing the charge density in the channel. This is essentially a surface-to-volume ratio argument and we expect, thus, an increased sensitivity for surface charges for smaller widths that should be reflected in a difference in threshold voltage with respect to width. A relevant scaling parameter for this effect to set in would be the thickness (here 100 nm). Indeed, Figure 2b shows I_{DS} vs V_{GS} curves for three nanowires of different size, confirming a threshold voltage dependence on nanowire width.

To further explore this effect, the threshold voltage has been extrapolated from the $I_{DS}-V_{GS}$ curves for nine nanowires of size ~50 to ~170 nm and one microwire of ~1 μm of width, as shown in Figure 3. The threshold voltage clearly decreases with increasing nanowire width, approaching a constant value at widths larger than ~150 nm. This is in agreement with the idea that the influence from surface charges is enhanced when the width of the nanowire is decreased.

This scenario is somewhat more complicated in reality because it is a well-known fact that a positive charge density is present at the silicon/silicon dioxide interface and also inside the oxide layer.[17] This charge will thus increase the conduction of the nanowire, assuming an electron channel. The fabrication process of the nanowires can also be assumed to give some nonzero surface charges surrounding the nanowire, which may be negative. If so, they will counteract the positive oxide charges and they will thus decrease the conductivity of the nanowire.

In the computer simulation, it is thus relevant to explore a scenario where both positive and negative charges are present at the surface. We have calculated the electron density over the two-dimensional cross section of a 100 nm wide nanowire and of a 1 μm wide microwire, both of 100 nm thickness. This is shown in Figure 4 for two different negative surface charge states where the less negative surface charge is indicated with repeated + and − signs. In the simulations, a positive interface charge density has been set to $+1 \times 10^{11}$ cm^{-2} at the bottom of the cross section as a realistic oxide charge.[17] The plots clearly demonstrate the effect of the negative charge at the surface, shrinking the channel toward the center of the channel, an effect which is more dramatic for the 100 nm wire.

To see the effect on the conductance, the cross sectional electron density has been integrated to get the conductance at the assumed surface charge according to:

$$G = \frac{q\mu_n}{L}\int_A n\,\mathrm{d}A$$

where L is the nanowire length, μ_n is the electron mobility (here set as 1000 cm^2/Vs as typical for an n-channel MOS transistor), q is the electron charge, and n is the electron density for each area element. This yields the conductance in the linear region (for small V_{DS}), far from pinch-off (note that serial resistance such as from the Schottky contact is not included in these calculations). The result is plotted in

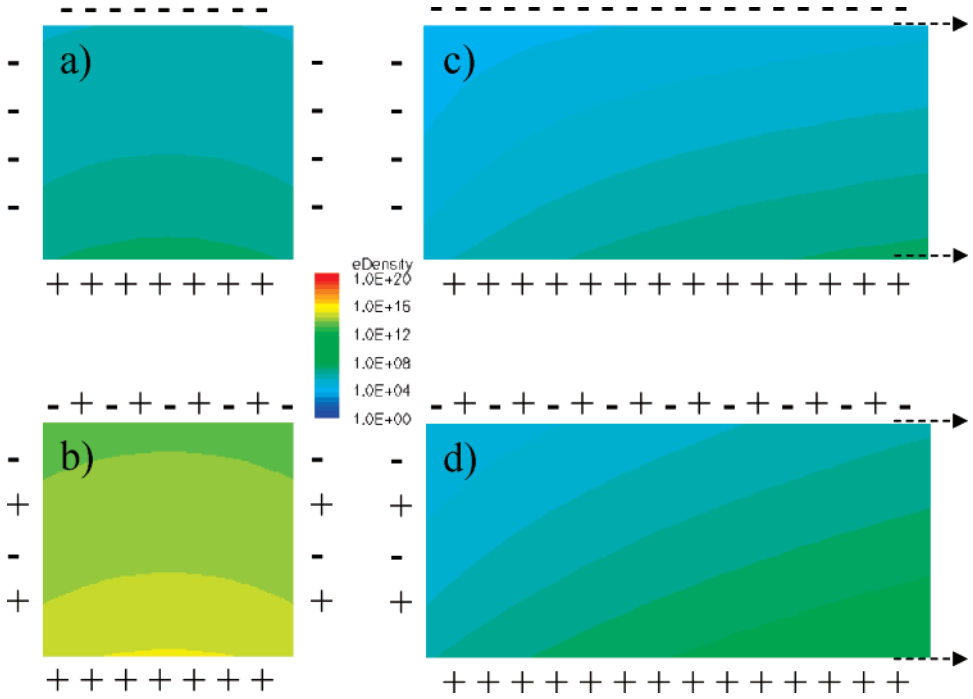

Figure 4. (a−b) Simulated electron concentration for a perpendicular cross section of a nanowire of 100 nm width. (c−d) Simulated electron concentration for the left 200 nm part of the microwire (1 μm total width) cross section. An assumed interface charge of $+1 \times 10^{11}$ cm^{-2} (in all cases) is indicated with repeated "+" signs at the bottom of both cross sections. For the nanowire, (a) illustrates the electron concentration at a surface charge of -3.2×10^{10} cm^{-2} indicated with repeated "−" signs while (b) shows the electron concentration at a surface charge of -3.1×10^{10} cm^{-2} indicated with repeated "+" and "−" signs. For the microwire, (c) illustrates the electron concentration at a surface charge of -9×10^{10} cm^{-2} indicated with repeated "−" signs while (d) shows the electron concentration at a surface charge of -8×10^{10} cm^{-2} indicated with repeated "+" and "−" signs.

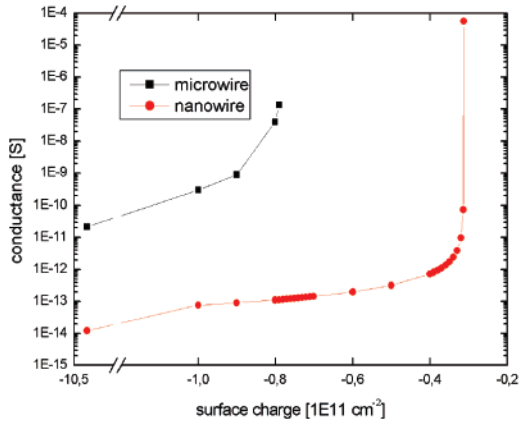

Figure 5. Calculated conductance vs surface charge for a nanowire of 100 nm width and a microwire of 1 μm width, both assuming an interface charge of $+1 \times 10^{11}$ cm^{-2}. The calculated conductance is based on integrations of perpendicular cross sections of simulated electron concentrations as shown in Figure 4.

Figure 5 versus surface charge for the two differently wide wires. Apparently, the conductance changes quite abruptly at a specific surface charge density, which is more positive for the nanowire due to the negative charge also at the side edges. Moreover, the rate of change in conductance per added surface charge is much larger for the nanowire than for the microwire. For instance, a change of only $\sim 6 \times 10^8$ cm^{-2} in surface charge close to the abrupt transition at $\sim -3 \times 10^{10}$ cm^{-2} induces a 10-fold increase in conductance (from $\sim 1 \times 10^{11}$ cm^{-2} to 1×10^{10} cm^{-2}). Assuming that such a change in conductance can be detected, we calculate that, for a 1 μm long and 100 nm wide nanowire (100 nm thick), this surface charge density corresponds to only ~2 elementary charges! Thus, the nanowire could in principle approach single-charge detection sensitivity (of course averaged on the time scale of binding/unbinding events at the surface).

These observations show that the presence of charges on the surface as well as interface properties have a large impact on these devices due to the large surface-to-volume ratio enabling efficient control of the induced channel. To further prove this, an experiment was designed to change the surface charges by the addition of a buffer solution. By adding a buffer solution of pH = 3 to the nanowire, the $-NH_2$ groups on the surface become positively charged and are protonated into $-NH_3^+$ groups and thus work as a positive top gate.[4] This enhances the current through the nanowire at a certain V_{DS}. Figure 6a shows the conductance shift at a certain V_{DS} for nanowires of different widths and a microwire when a buffer solution is added to the surface of the wire. In accordance with previous results, the smallest nanowire reacts more to the surface charge change than the microwire, whose conductance remains constant. In another experiment, the buffer solution was changed from one with pH = 3.0 to one with pH = 7.4. This resulted in large threshold voltage shifts for the smaller wires, but essentially no difference was observed for nanowires larger than ~150 nm (see Figure 6b). Note that in these experiments contacts were protected from the buffer solution by a polymer, and only the nanowire was exposed to the different solutions (see Supporting Information).

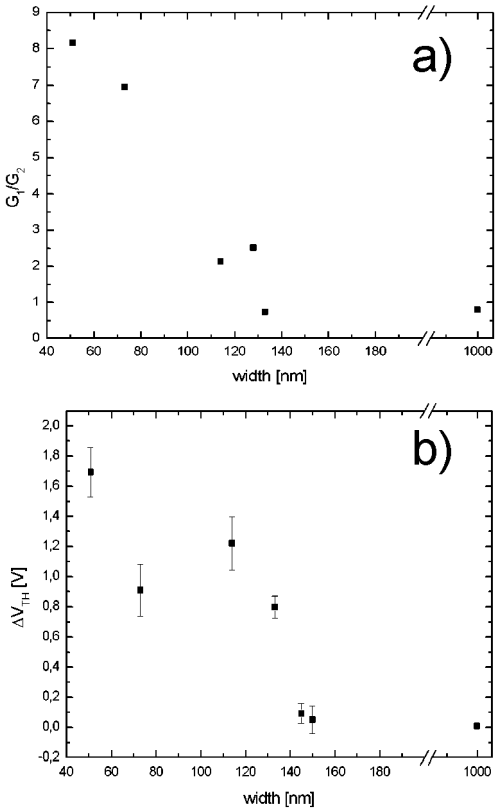

Figure 6. (a) Conductance ratio vs width for nanowires in the range ~50−100 nm and for a microwire at $V_{DS} = 0.65$ V. Here the shift occurred when the bare surface was covered with a buffer solution of pH = 3.0. (b) Threshold voltage shift, ΔV_{TH}, vs width for nanowires in the range ~50−100 nm and for a microwire of ~1 μm width at $V_{DS} = 0.65$ V. The shift occurred when the pH value of the buffer solution added to the surface was changed from 3.0 to 7.4.

These data clearly show that the impact of surface charges is dependent on the surface-to-volume ratio and that this can explain the increasing threshold voltage for decreasing nanowire width and confirms the simulations and theory. For nanowires of larger width than ~150 nm, the behavior is similar to that of the microwires and no detection sensitivity seems to be left.

Summarizing, we have shown that the threshold voltage increases, due to an increasing surface charge effect, with decreasing nanowire width. This effect has been demonstrated through computer simulation and experimentally for an oxide-covered nanowire and microwire surface and for surfaces exposed to buffer solutions of pH = 3.0 and 7.4. This shows that the silicon nanowire could work as a sensitive detector for sensing pH and charged molecules attached to the surface down to the single-charge level. We also demonstrate that extraction of the threshold voltage is a promising way of characterizing changes of the surface charge. Finally, large nanowires with widths >~150 nm lose their detection sensitivity similarly to micrometer-sized wires.

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Supporting Information Available: $I_{DS}-V_{DS}$ characteristics for several nanowires and a microwire and pH experiment preparation. This material is available free of charge via the Internet at http://pubs.acs.org.

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